CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence (along with any paper referred to as being attached or enclosed) is being submitted *via* the USPTO EFS Filing System on the date shown below to **Mail Stop Appeal Brief - Patents**, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Date: October 4, 2006 /Jessica Sexton/
Jessica Sexton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:			
Appellants:	Ming-Huei Shieh, *et al.*	Examiner:	Dang T. Nguyen
Serial No:	10/600,065	Art Unit:	2824
Filing Date:	June 20, 2003		

Title: MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

Appellants' submits this brief in connection with an appeal of the above-identified patent application. Payment is being submitted via credit card in connection with all fees due regarding this appeal brief. In the event any additional fees may be due and/or are not covered by the credit card, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1063 [AMDP975US].

I. Real Party in Interest (37 C.F.R. §41.37(c)(1)(i))

The real party in interest in the present appeal is Spansion LLC, the assignee of the present application.

II. Related Appeals and Interferences (37 C.F.R. §41.37(c)(1)(ii))

Appellants, appellants' legal representative, and/or the assignee of the present application are not aware of any appeals or interferences which may be related to, will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. §41.37(c)(1)(iii))

Claims 1-4 and 6-27 stand rejected by the Examiner. The rejection of claims 1-4 and 6-27 is being appealed. Claim 5 has been cancelled.

IV. Status of Amendments (37 C.F.R. §41.37(c)(1)(iv))

The Examiner has not entered the amendments submitted after the Final Office Action. (*See* Advisory Action from Examiner dated Aug. 18, 2006).

V. Summary of Claimed Subject Matter (37 C.F.R. §41.37(c)(1)(v))

A. Independent claim 1

Independent claim 1 recites an architecture that facilitates a reference voltage in a multi-bit memory. The architecture first comprises a multi-bit memory core 401 including a plurality of data cells for storing data. The architecture further comprises first and second reference arrays (408 and 410) of a plurality of multi-bit reference cells fabricated on the memory core 401, with pairs of the multi-bit reference cells each associated with separate wordlines within the multi-bit memory core 401. By fabricating the reference cells on the memory core 401, referencing can be performed dynamically among a number of different multi-bit reference pairs. Claim 1 further recites a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage employed during a data cell read operation. (*See, e.g.* Figure 12, and corresponding text, page 18, line 25 – page 20, line 9).

B. Dependent claim 11

Dependent claim 11 recites the architecture of claim 1, the first and second reference arrays including corresponding reference cells that are interweaved among the data cells. By interweaving the reference cells amongst the data cells, for example, claim 11 provides increased reference voltage accuracy with respect to data bit values of the data cell sectors. (*See, e.g.* Figure 9 and corresponding text at page 16, lines 3-11).

C. Independent claim 13

Independent claim 13 recites an architecture that facilitates a reference voltage in a multi-bit memory, comprising a multi-bit memory core 401 for storing data, the memory core 401 including two groups of data sectors (404, 406). The architecture further comprises first and second reference arrays (408, 410) of a plurality of multi-bit reference cells fabricated on the memory core interstitial to the groups of data sectors (404, 406), with pairs of the plurality of multi-bit reference cells each associated with a disparate wordline within the two groups of data sectors; and a first bit value of a first reference cell of the first reference array and a second bit value of a second reference cell of the second reference array forming a reference pair whose respective bit values are averaged to arrive at the reference voltage for a read operation. (*See, e.g.* Figure 12, and corresponding text, page 18, line 25 – page 20, line 9).

D. Independent claim 17

Independent claim 17 recites a method for providing a reference voltage in a multi-bit memory, comprising receiving a multi-bit memory core for storing data, providing first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core and associating pairs of the plurality of multi-bit reference cells each with separate wordlines within the memory core. Moreover, an averaging procedure takes place wherein averaging of a first bit value of a first reference cell of the first reference array with a second bit value of a second reference cell of the second reference array occurs to arrive at the reference voltage utilized during a read operation (at 340). (*See, e.g.* Figure 11, and corresponding text, page 17, line 14 – page 18, line 24).

E. Independent claim 24

Independent claim 24 recites a system for providing a reference voltage in a multi-bit memory. The system initially comprises means for providing a multi-bit memory core for storing data (*See, e.g.* Figure 12, and corresponding text, page 18, lines 25 – 29). The system further comprises means for providing first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core (*See, e.g.* Figure 12, and corresponding text, page 18, line 30 – page 19, line 16). Moreover, the system provides means for averaging a first bit value of a first reference cell of the first reference array with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage to facilitate a read operation (*See, e.g.* Figure 11, and corresponding text, page 18, lines 4 – 7). In addition, the system comprises means for separately monitoring process variations at each wordline within the multi-bit memory core (*See, e.g.* Figure 8, and corresponding text at page 15, line 10 – page 16, line 2).

The aforementioned means for limitations are identified as claim elements subject to the provisions of 35 U.S.C. §112 ¶6. The corresponding structures are identified with reference to the specification and drawings in the parentheticals above corresponding to those claim limitations.

F. Dependent claim 25

Claim 25 recites the system of claim 24, the first and second reference arrays including corresponding reference cells that are interweaved among the data cells. By interweaving the reference cells amongst the data cells, for example, claim 25 provides increased reference voltage accuracy with respect to data bit values of the data cell sectors. (*See, e.g.* Figure 9 and corresponding text at page 16, lines 3-11).

VI. Grounds of Rejection to be Reviewed on Appeal (37 C.F.R. §41.37(c)(1)(vi))

A. Whether claims 1-4 and 6-12 fail to comply with the written description requirement under 35 U.S.C §112, first paragraph.

B. Whether claims 1-4 and 6-23 are indefinite under 35 U.S.C. §112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

C. Whether claims 1-4, 6-14 and 17-26 are anticipated under 35 U.S.C. §102(e) by Le *et al.* (US 6,690,602).

D. Whether claims 16 and 27 are unpatentable under 35 U.S.C. §103(a) over Le *et al.* in view of Kurihara *et al.* (US 6,791,880).

E. Whether claim 15 is unpatentable under 35 U.S.C. §103(a) over Le *et al.* in view of Ferrant (US 6,538,942).

VII. Argument (37 C.F.R. §41.37(c)(1)(vii))

A. Rejection of Claims 1-4 and 6-12 Under 35 U.S.C §112

Claims 1-4 and 6-12 stand rejected under 35 U.S.C §112, first paragraph, as failing to comply with the description requirement. This rejection should be reversed for at least the following reasons. Pursuant to 37 C.F.R. §1.116 (b)(1), after final action, "An amendment may be made canceling claims or ***complying with any requirement of form expressly set forth in a previous Office Action***…". The amendments to independent claim 1 to address this rejection in the Reply to the Final Office Action (dated April 4, 2006) were made in response to this newly raised rejection in the Final Office Action. Moreover, the amendment to independent claim 1 is commensurate with the Examiner's interpretation for examination purposes as stated in the Final Office Action, and supported in the instant specification at page 15, line 13 - page 16, line 2 and corresponding Figure 8. Accordingly, reversal of this rejection is respectfully requested in view the amendment in the Reply to Final Office Action that addresses this rejection.

B. Rejection of Claims 1-4 and 6-23 Under 35 U.S.C §112

Claims 1-4 and 6-23 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. This rejection should be reversed for at least the following reasons. Pursuant to 37 C.F.R. §1.116 (b)(1), the amendments to independent claims 1, 13 and 17 in response to this newly raised rejection in the Final Office Action should have been entered by the Examiner. Therefore, this rejection should be reversed.

C. Rejection of Claims 1-4, 6-14 and 17-26 Under 35 U.S.C. §102(e)

Claims 1-4, 6-14 and 17-26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Le *et al.* (US 6,690,602). This rejection should be reversed for at least the following reasons. Le *et al.* does not disclose all features of the subject claims.

> A single prior art reference anticipates a patent claim only if it ***expressly or inherently describes each and every limitation set forth in the patent claim***. *Trintec Industries, Inc. v. Top-U.S.A. Corp.,* 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). ***The identical invention must be shown in as complete detail as is contained in the ... claim***. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

The claimed invention relates to on-chip placement of referencing circuitry in a multi-bit memory device. In particular, Independent claim 1 recites an architecture that facilitates a reference voltage in a multi-bit memory, comprising a multi-bit memory core including a plurality of data cells for storing data; ***first and second reference arrays of a plurality of multi-bit reference cells fabricated on the memory core***, pairs of the plurality of the multi-bit reference cells each associated with separate wordlines within the multi-bit memory core; and a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array ***to arrive at the reference voltage employed during a data cell read operation***. Independent claims 13, 17 and 24 recite similar features. Le *et al.* does not disclose such aspects of the subject claims.

Le *et al*. relates to a system having a memory cell array and associated reference arrays. At page 5 of the Final Office Action, the Examiner incorrectly contends that Le *et al.* teaches that the *first and second reference arrays of a plurality of multi-bit reference cells are* ***fabricated on the memory core***, as in the claimed invention. At the indicated portions, Le *et al.* teaches that reference arrays are associated with an adjacent sector of memory cells; however, Le *et al.* does not disclose that reference cells of the first and second reference arrays are fabricated on the memory core along with the sector of memory cells. Consequently, for example, Le *et al.* does not provide referencing capabilities that can be performed dynamically among a number of different multi-bit reference pairs of the memory core, as afforded by the claimed aspect of

fabricating reference cells ***on the memory core***.

Moreover, the Examiner incorrectly contends that the cited reference teaches a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array ***to arrive at the reference voltage employed during a data cell read operation.*** To the contrary, Le *et al.* averages voltage levels of core and reference cells to effectuate programming and erasing within the memory cells. On the other hand, for example, the claimed invention employs the reference voltage derived from the averaging procedure to ascertain whether a data bit from a memory cell is programmed or unprogrammed. Therefore, Le *et al.* does not employ the reference voltage during a data cell read operation; rather, Le *et al.* utilizes the average voltage to facilitate erase procedures in memory cells. Thus, Le *et al.* does not disclose that the average reference voltage is ***employed during a data cell read operation***, as afforded by the claimed invention.

Furthermore, claims 11 and 25 recite similar features, namely ***the first and second reference arrays including corresponding reference cells that are interweaved among the plurality of data cells.*** On page 7 of the Final Office Action, the Examiner incorrectly asserts that Figure 4 of Le *et al.* teaches the features recited in claims 11 and 25. Le *et al.* teaches a core cell and two reference cells, and further discloses that data from the core cell is compared to an average value of the two reference cells during programming/erase verification procedures. However, Figure 4 of Le *et al.* does not address the placement of the reference cells amongst the core cells. The cited reference further shows a sector of core cells and two reference arrays (*See* Figure 3). While both the core cell sector and the reference arrays include multi-bit data cells, the reference does not teach that data cells of the reference arrays are interweaved amongst the core cells. Therefore, Le *et al.* does not afford the increased reference voltage accuracy with respect to data bit values of the data cell sectors as the claimed invention provides with ***the first and second reference arrays including corresponding reference cells that are interweaved among the plurality of data cells***.

What is more, independent claim 13 further recites first and second reference arrays of a plurality of multi-bit reference cells ***fabricated on the memory core interstitial to two groups of data sectors***. Le *et al.* does not provide such an arrangement; instead, as noted above, while Le *et al.* shows a sector of core data cells associated with two reference arrays with corresponding reference cells, the cited reference does not disclose that the reference cells are fabricated on the

memory core. Consequently, Le *et al.* further does not disclose that the reference cells are ***fabricated on the memory core and interstitial to two groups of data sectors*** on the memory core, as afforded by independent claim 13.

In view of at least the foregoing, it is readily apparent that Le *et al.* does not teach the identical invention in as complete detail as is contained in the subject claims. Accordingly, this rejection with respect to independent claims 1, 13, 17 and 24 (and the claims that depend from) should be withdrawn.

D. Rejection of Claims 16 and 27 Under 35 U.S.C. §103(a)

Claims 16 and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Le *et al.* in view of Kurihara *et al.* (US 6,791,880). Applicants' representative respectfully requests reversal of this rejection for at least the following reasons. The subject claims depend from independent claims 13 and 24. As discussed above, Le *et al.* does not teach or suggest appellants' invention as recited in such independent claims; and Kurihara *et al.* does not make-up for the aforementioned drawbacks of the primary reference. Accordingly, this rejection should be reversed.

E. Rejection of Claim 15 Under 35 U.S.C. §103(a)

Claim 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Le *et al.* in view of Ferrant (US 6,538,942). This rejection should be reversed for at least the following reasons. The subject claim depends from independent claim 13. As noted above, Le *et al.* does not disclose or suggest all features of independent claim 13, and Ferrant does not compensate for the drawbacks of the primary reference. Therefore, reversal of this rejection is respectfully requested.

F. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 1-4 and 6-27 be reversed.

If any additional fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP975US].

Respectfully submitted,

AMIN, TUROCY & CALVIN, LLP

/Himanshu S. Amin/
Himanshu S. Amin
Reg. No. 40,894

AMIN, TUROCY & CALVIN, LLP
24TH Floor, National City Center
1900 E. 9TH Street
Cleveland, Ohio 44114
Telephone (216) 696-8730
Facsimile (216) 696-8731

VIII. Claims Appendix (37 C.F.R. §41.37(c)(1)(viii))

1. An architecture that facilitates a reference voltage in a multi-bit memory, comprising:

a multi-bit memory core including a plurality of data cells for storing data;

first and second reference arrays of a plurality of multi-bit reference cells fabricated on the memory core, the plurality of multi-bit reference cells each associated with separate wordlines within the multi-bit memory core; and

a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage employed during a data cell read operation.

2. The architecture of claim 1, the core further comprising a sector of multi-bit data cells organized in rows and columns with associated wordlines attached to the multi-bit data cells in a row and with associated bitlines attached to the multi-bit data cells in a column, the first and second reference cells forming a multi-bit reference pair that is programmed and erased with the multi-bit data cells during programming and erase cycles.

3. The architecture of claim 2, the multi-bit reference pair is associated with a word in a wordline, the multi-bit reference pair utilized during reading of bits of the word.

4. The architecture of claim 2, the multi-bit reference pair is associated with multi-bit data cells in a wordline, the multi-bit reference pair utilized during reading of bits in the wordline.

5. (Cancelled)

6. The architecture of claim 2, the multi-bit reference pair is associated with multi-bit data cells in the sector, the multi-bit reference pair utilized during reading of bits in the sector.

7. The architecture of claim 1, the memory core including a plurality of data sectors that are accessible by the first and second reference arrays, the first and second reference arrays located centrally of the plurality of data sectors.

8. An integrated circuit comprising the memory of claim 1.

9. A computer comprising the memory of claim 1.

10. An electronic device comprising the memory of claim 1.

11. The architecture of claim 1, the first and second reference arrays including corresponding reference cells that are interweaved among the data cells.

12. The architecture of claim 1, the memory core further comprising a plurality of data sectors, such that each data sector is associated with at least one of the first reference array and the second reference array of multi-bit reference cells.

13. An architecture that facilitates a reference voltage in a multi-bit memory, comprising:

a multi-bit memory core for storing data, the memory core including two groups of data sectors;

first and second reference arrays of a plurality of multi-bit reference cells fabricated on the memory core interstitial to the groups of data sectors, the plurality of the reference pairs each associated with a disparate wordline within the two groups of data sectors; and

a first bit value of a first reference cell of the first reference array and a second bit value of a second reference cell of the second reference array forming a reference pair whose respective bit values are averaged to arrive at the reference voltage for a read operation.

14. The architecture of claim 13, the groups of data sectors read in an interleaved manner with a selected reference pair.

15. The architecture of claim 13, the first and second reference arrays precharged before being averaged.

16. The architecture of claim 13, further comprising a redundancy array located at least one of proximate and adjacent to the groups of data sectors.

17. A method for providing a reference voltage in a multi-bit memory, comprising:

receiving a multi-bit memory core for storing data;

providing first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core;

associating each of the plurality of multi-bit reference pairs with separate wordlines within the memory core; and

averaging a first bit value of a first reference cell of the first reference array with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage utilized during a read operation.

18. The method of claim 17, the core comprising a sector of multi-bit data cells organized in rows and columns with associated wordlines attached to the multi-bit data cells in a row and with associated bitlines attached to the multi-bit data cells in a column, the multi-bit reference pairs are programmed and erased with the multi-bit data cells during programming and erase cycles.

19. The method of claim 18, the multi-bit reference pair is associated with a word in a wordline, the multi-bit reference pair utilized during reading of bits in the word.

20. The method of claim 18, the multi-bit reference pair is associated with multi-bit data cells in a wordline, the multi-bit reference pair utilized during reading of bits in the wordline.

21. The method of claim 18, the associated multi-bit reference pair utilized during reading of bits in the corresponding wordline.

22. The method of claim 18, the multi-bit reference pair is associated with multi-bit data cells in the sector, the multi-bit reference pair utilized during reading of bits in the sector.

23. The method of claim 17, the memory core including a plurality of data sectors that are accessible by the first and second reference arrays, the first and second reference arrays located centrally of the plurality of data sectors.

24. A system for providing a reference voltage in a multi-bit memory, comprising:

means for providing a multi-bit memory core for storing data;

means for providing first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core; and

means for averaging a first bit value of a first reference cell of the first reference array with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage to facilitate a read operation; and

means for separately monitoring process variations at each wordline within the multi-bit memory core.

25. The system of claim 24, the first and second reference arrays including corresponding reference cells that are interweaved among the data cells.

26. The system of claim 24, the memory core further comprising a plurality of data sectors, such that each data sector is associated with at least one of the first reference array and the second reference array of multi-bit reference cells.

27. The system of claim 24, further comprising a redundancy array located at least one of proximate and adjacent to the groups of data sectors.

IX. Evidence Appendix (37 C.F.R. §41.37(c)(1)(ix))

None.

X. Related Proceedings Appendix (37 C.F.R. §41.37(c)(1)(x))

None.